REMARKS

Claims 1-4, 11 and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Borchers, *et al.* (U.S. Publication Number 2004/0044934). Claims 7 and 9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Moloney, *et al.* (U.S. Patent Number 5,528,237). Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Borchers, *et al.* in view of Kubota, *et al.* (U.S. Patent Number 5,654,658). Claims 8 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Moloney, *et al.* in view of Kubota, *et al.* In view of the amendments to the claims and the following remarks, the rejections of claims 7, 8 and 10 are respectfully traversed, and reconsideration of the rejections is requested.

Regarding the rejections of claims 1-4, 11 and 12 under 35 U.S.C. § 102(e) and of claims 5 and 6 under 35 U.S.C. § 103(a), the claims are cancelled.

The present invention as claimed in claims 7, 8 and 10 is directed to a control signal generation circuit used in controlling memory access through memory addressing. One control signals is a column latch signal COLLAT, and another control signal is a data input/output command signal COLCYC. The column latch signal COLLAT is output at a first output terminal of the circuit, and the data input/output command signal COLCYC is output at a second output terminal of the circuit. A first latch latches an input signal in response to a clock signal. The first latch outputs an output signal to be output as the column latch COLLAT signal. The first latch further outputs the output signal to an input terminal of a second latch.

The claims are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the first latch outputs the output signal to the first output of the control signal generator and to the input terminal of the second latch. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Moloney, *et al.* discloses that an output value Z of a first combinative logic network RC1 is fed to a D input of a first flip-flop C, which is sampled by a base clock signal VCO. An output of the flip-flop C is fed to a D input of a first latch in flip-flop DD. The output of the first latch in flip-flop DD is fed to a second latch in the flip-flop DD and to an input of a selection

multiplexer 2-1 MUX. The output of the second latch in the flip-flop DD is fed to an input of the selection multiplexer 2-1 MUX (see Moloney, *et al.*, FIG. 6).

Moloney, *et al.* fails to teach or suggest that a first latch outputs an output signal to a first output of a control signal generator and to an input terminal of a second latch. Instead, in Maloney, *et al.*, the flip-flop C outputs a signal only to the first latch of the flip-flop DD, and thus does not output a signal to an output of a control signal generator.

Hence, Moloney, *et al.* fails to teach or suggest certain elements of the invention set forth in the amended claims. Specifically, Moloney, *et al.* fails to teach or suggest that a first latch outputs an output signal to a first output of a control signal generator and to an input terminal of a second latch. Therefore, it is believed that claim 7 is allowable over Moloney, *et al.* Accordingly, reconsideration of the rejections of claim 7 under 35 U.S.C. § 102(b) based on Moloney, *et al.* is respectfully requested.

Kubota, *et al.* discloses a flip-flop circuit including a master circuit constructed with a feedback-loop type flip-flop circuit consisting of inverters 3, 8 and transfer gates 2, 7 (see Kubota, *et al.*, FIG. 15A). Kubota, *et al.* fails to teach or suggest that a first latch outputs an output signal to a first output of a control signal generator and to an input terminal of a second latch.

Hence, neither of Moloney, *et al.* and Kubota, *et al.* teaches or suggests certain elements of the present invention set forth in amended claims 7, 8 and 10. Specifically, neither of the references teaches or suggests that a first latch outputs an output signal to a first output of a control signal generator and to an input terminal of a second latch, as claimed in amended claims 7, 8 and 10. Accordingly, there is no combination of the references which would provide such teaching or suggestion.

Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in the amended claims. Therefore, it is believed that the amended claims are allowable over the cited references, and reconsideration of the rejections of claims 8 and 10 under 35 U.S.C. § 103(a) based on Moloney, *et al.* and Kubota, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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